SPECIFICATION AMENDMENTS

Replace the paragraph beginning at page 1, line 10 with:

Fig. 12 is a schematic top view for illustrating an interconnecting structure in a conventional semiconductor device. Fig. 13 is a sectional view taken along the line ~~F—F'~~ XIII-XIII of Fig. 12 showing the interconnecting structure manufactured using a dual damascene method.

Replace the paragraph beginning at page 1, line 22 with:

In recent years, the miniaturization of semiconductor devices has caused an accompanying problem of wiring signal delay. In order to solve such a problem, copper (Cu) is used as a wiring material, and a low-k dielectric film having a low dielectric constant (k) is used as interlayer dielectric films (for example, refer to Non-Patent Document "K. ~~Hayashi~~ Higashi et al., Proceedings of the 2002 International Interconnect Technology Conference, pp. 15-17").

Replace the paragraph beginning at page 1, line 29 with:

However, when a dimension of vias is reduced, density difference between isolated vias and dense vias is enlarged due to the proximity effect. Furthermore, when vias are formed using a low-k dielectric film as an interlayer dielectric film, and when a chemically amplified resist, such as a KrF resist and an ArF resist, is used as a mask, the problems of via resistance elevation and the occurrence of wire breaking are caused, in particular in isolated vias, by an acid of the chemically amplified resist. In other words, a problem of the occurrence of a phenomenon known as "resist poisoning" arises in vias, in particular in isolated vias. These problems are often caused when a cap film including different insulating films is formed on a low-k dielectric film in order to prevent ~~causing~~ ashing damage to the low-k dielectric film.

Replace the paragraph beginning at page 3, line 12 with:

Figs. 2A and 2B are sectional views taken along the line ~~A—A'~~ II-II of Fig. 1 showing the interconnecting structure manufactured using a dual damascene method;

Replace the paragraph beginning at page 3, line 21 with:

Fig. 5 is a sectional view taken along the line ~~B—B'~~ V-V of Fig. 4 showing the interconnecting structure manufactured using a dual damascene method;

Replace the paragraph beginning at page 3, line 27 with:

Fig. 7 is a sectional view taken along the line ~~C—C'~~ VII-VII of Fig. 6 showing the interconnecting structure manufactured using a dual damascene method;

Replace the paragraph beginning at page 4, line 1 with:

Fig. 9 is a sectional view taken along the line ~~D—D'~~ IX-IX of Fig. 8 showing the interconnecting structure manufactured using a dual damascene method;

Replace the paragraph beginning at page 4, line 7 with:

Fig. 11 is a sectional view taken along the line ~~E—E'~~ XI-XI of Fig. 10 showing the interconnecting structure manufactured using a dual damascene method;

Replace the paragraph beginning at page 4, line 13 with:

Fig. 13 is a sectional view taken along the line ~~F—F'~~ XIII-XIII of Fig. 12 showing the interconnecting structure manufactured using a dual damascene method.

Replace the paragraph beginning at page 4, line 25 with:

Fig. 1 is a schematic top view ~~for~~ illustrating an interconnecting structure in a semiconductor device according to a first embodiment of the present invention. Figs. 2A and 2B are sectional views taken along the line ~~A—A'~~ II-II of Fig. 1 showing the interconnecting structure manufactured using a dual damascene method.

Replace the paragraph beginning at page 9, line 10 with:

Fig. 4 is a schematic top view ~~for~~ illustrating an interconnecting structure in a semiconductor device according to a second embodiment of the present invention. Fig. 5 is a sectional view taken along the line ~~B—B'~~ V-V of Fig. 4 showing the interconnecting structure manufactured using a dual damascene method.

Replace the paragraph beginning at page 10, line 17 with:

Fig. 8 is a schematic top view ~~for~~ illustrating an interconnecting structure in a semiconductor device according to a fourth embodiment of the present invention. Fig. 9 is a sectional view taken along the line ~~D—D'~~ IX-IX of Fig. 8 showing the interconnecting structure manufactured using a dual damascene method.

Replace the paragraph beginning at page 11, line 4 with:

Fig. 10 is a schematic top view ~~for~~ illustrating an interconnecting structure in a semiconductor device according to a fifth embodiment of the present invention. Fig. 11 is a sectional view taken along the line ~~E—E'~~ XI-XI of Fig. 10 showing the interconnecting structure manufactured using a dual damascene method.